CLAIMS:

1. (Original): A system to provide software program control of cache management, comprising:

a processor configured to generate DMA commands for the management of a cache on the execution of a software program on the processor; and

a DMA controller coupled to the processor, configured to execute the DMA commands for the management of a cache.

2. (Original): The system of Claim 1, further comprising a cache coupled to the DMA controller, the system configured for the execution of the DMA commands for the management of a cache on the DMA controller to manage the operation of the cache coupled to the DMA controller.

3. (Original): The system of Claim 1, wherein at least one of the DMA commands is a get command and at least one of the DMA commands is a put command.

4. (Original): The system of Claim 1, wherein at least one of the DMA commands is a flush command.

5. (Original): The system of Claim 1, wherein at least one of the DMA commands is a zero command.

6. (Currently Amended): The system of Claim 1, wherein the parameters of the DMA commands comprise ~~class line,~~ tag, transfer size, and effective address low.

7. (Original): The system of Claim 1, wherein the cache is a DMA cache tightly coupled to the DMA controller.

8. (Original): The system of Claim 1, wherein the cache is a cache for system memory.

9. (Original): A method for cache management in a system comprising a DMA controller and a processor, the method comprising the steps of:

running software on the processor to generate DMA commands for management of a cache;

issuing the DMA commands to the DMA controller; and

executing the DMA commands.

10. (Original): The method of Claim 9, wherein a cache is coupled to the DMA controller, and executing the DMA commands on the DMA controller manages the operation of the cache.

11. (Original): The method of Claim 9, wherein at least one of the DMA commands is a put command and wherein at least one of the DMA commands is a get command.

12. (Original): The method of Claim 9, wherein at least one of the DMA commands is a flush command.

13. (Original): The method of Claim 9, wherein the cache is a DMA cache tightly coupled to the DMA controller.

14. (Original): The method of Claim 9, wherein the cache is a cache for system memory.

15. (Original): A computer program product for cache management in a system comprising a DMA controller and a processor, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for running software on the processor to generate DMA commands for management of a cache;

computer code for issuing the DMA commands to the DMA controller; and

computer code for executing the DMA commands.

16. (Original): The computer program product of Claim 15, wherein at least one of the DMA commands is a get command.

17. (Original): The computer program product of Claim 15, wherein at least one of the DMA commands is a put command.

18. (Original): The computer program product of Claim 15, wherein at least one of the DMA commands is a flush command.

19. (Original): The computer program product of Claim 15, wherein at least one of the DMA commands is a zero command.

20. (Original): The computer program product of Claim 15, wherein the cache is a DMA cache tightly coupled to the DMA controller.

21. (Original): The computer program product of Claim 15, wherein the cache is a cache for system memory.